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Development of PEF source in Nanosecond range for Food Sterilization

Pulsed Electric Field [PEF] food processing technology becomes more attractive, alternative to thermal food processing technologies. Usually the high voltage pulses are generated using conventional pulse generators based on Marx cells, Spark gaps, Electrostatic filters to produce the necessary high electric filed intensity. The voltage and current are limited due to the classical switches used in the conventional generators. The switching speed and slow response of such devices increase the complexity of the control and driver circuits and also the space requirement of the conventional generators. The drawbacks of pulse generators are overcome by the advanced semiconductor devices, such as power MOSFETs and are becoming most suitable for high speed switching high voltage pulse generators. The modern semiconductor devices are more reliable to handle high voltages and currents when implemented in typical circuits and reduces the bulkiness of the High Voltage Pulse Generator [HVPG]. This paper proposes the developments in HVPG using modern semiconductor devices. The energy efficiency can be improved by minimizing the losses during food process and it can be achieved by reducing the pulse width using modern semiconductors. The proposed generators are capable of producing high voltage sub-microseconds pulses in the range of 100ns to few microseconds.

Keywords: Power MOSFETs; electroporation; inactivation of microorganisms; IFR740 MOSFET.

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1. Introduction

In recent years, PEF finds applications in many fields that require instant high power like Food Processing, Waste treatment, Gene Therapy, Cell fusion, Drug delivery and Cancer treatment [1-14].In particular, PEFs used in food processing can provide high quality food. PEF method maintains the taste, colour, flavour and the nutritional value of the food. The physical and structural characteristics are degraded by the thermal food processing methods. So, PEF can complement the conventional thermal processing methods. This method can be used for liquid and semi liquid foods. The food processing method by PEF means inactivating the microbes which are presented in the liquid foods and improving the shelf life of foods. Figure 1 shows the equivalent model of a microbe inside the suspension which describes about the concept cell interaction with electric field. The PEF method involves the application of high electric field intensity in the range of few kV/cm across certain electrode geometry that contains the liquid food [21].

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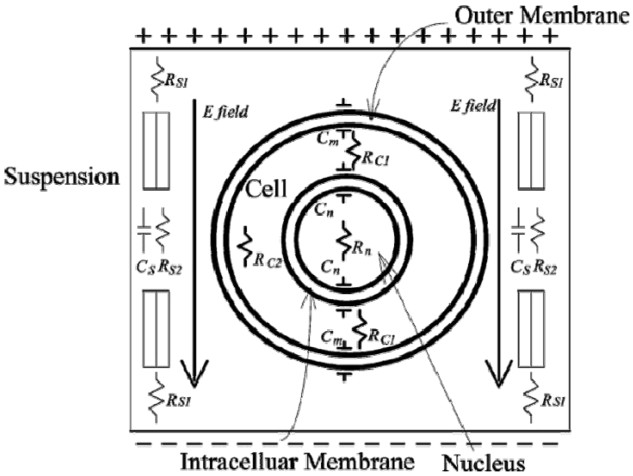

Figure 1. Equivalent model of a cell inside suspension [6]

Before PEFs are applied to a microbial cell, liquid food surrounds the outside of the cell membrane, while cytoplasm stays inside the cell. If the voltage across the microbial cell membrane is higher than 1 V when it is subjected to strong brief high voltage pulses, irreversible pores are created over the membrane. Then liquid molecules will flow into the cell through the pores. When the repetitive rate and pulse width are large enough, the cell membrane will be ruptured and the cytoplasm will flow outside the cell [8], [9]. This process is called electroporation and is shown in Figure 2 [9]. Finally, the cell is destroyed. Narrow pulses are usually used to generate apoptosis in microbe processing. Apoptosis is a series of natural enzymatic reactions, which have evolved for the natural elimination of unhealthy, genetically damaged, or aberrant cells [7], [10]. As a result, it needs high-power and high-voltage pulse generators to achieve the microbial inactivation [15]–[20].

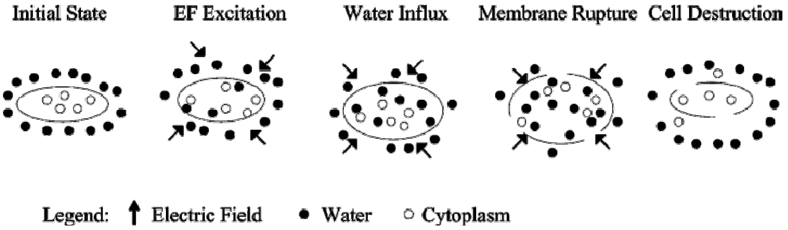

Figure 2. Illustration of electroporation procession of a cell [9]

The membrane potential V_m is given as equation (1)[21],

$$V_m = 1.5Ea\cos\delta \tag{1}$$

Where ‘a’ is the cell radius, and ‘δ’ is the angle between the electric field ‘E’ and the radius vector of cell. In general the cell dimension is approximately taken as 10 μm and cosδ to be 1, then the resulting field strength becomes 1 kV/cm[21].

The conventional PEF sources are used in practice as non- thermal food processing technique and the typical PEF source is shown in Figure 3. A Capacitor bank is charged using a High Voltage DC source. After it gets charged to sufficiently high level with a time constant of $\tau = RC$, the discharge switch is closed at a high switching frequency. The food treatment chamber consists of two parallel plate electrodes and HV pulses are applied across the electrodes, thereby producing Sub-Microscopic Pulsed Electric Field. The electric field strength can be adjusted by varying the distance between the electrodes and the gap distance is 1mm-5mm for small scale application to increase the electric field intensity.The literature survey on electroporation shows that square pulses are most effective in inactivation of microbes than exponential decay and oscillatory pulses. The square pulses varying from few kilovolts/cm to 100 kilovolts/cm with millisecond to nanosecond pulse widths have been successfully used [2, 3, 6].

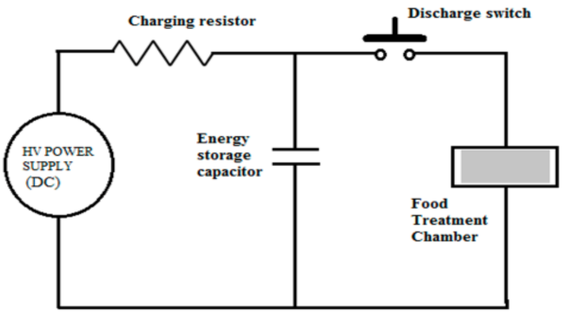

Figure 3. Typical PEF source

The conventional PEF sources use Ignitron, thyratron, tetrode, spark gap as the discharge switch to deliver the high intensity pulses. The drawbacks of the classical switches are i) the Repetition rate is limited ,<100Hz, ii) Complexity in designing the triggering circuits is more, iii) Rise time and fall time are increased and alters the wave-shape, iv) Thyratron switches are limited regarding the maximum energy delivered per pulse. Many attempts are being made to counter these shortcomings.

The improved versions of solid state switches like SCR (Silicon Controlled Rectifier), GTO (Gate Turn-off) or IGBT (insulated Gate Bipolar Transistor) require less complex driving circuits and are easy to handle and control by external triggering and optimum variability of pulse parameters. Pulse repetition of standard switches can reach up to several kHz, suitable for application in industrial scale.

Thus, solid-state devices such as MOSFETs are gaining momentum as candidates for high speed, fast switching of high voltages of several hundred volts required for pulsed applications, including Bio-Technology and medical applications [22-26]. This paper proposes a new PEF source based on advanced semiconductor power MOSFETs. These generators use such components that withstand very high instantaneous voltage, current and very high switching frequencies at reduced rate. This paper presents the simulation of HVPG design based on power MOSFETs IRF740.

2. Circuit Description of Series Connected MOSFET - IRF740

A pulse generator that is capable of reliably generating the required pulses is an integral part of the electroporation therapy. The improvements in solid state devices make the pulse generator as simple and inexpensive when compared to conventional HVPG. Many solid state devices are available in the market. Manufacturers give specifications to assist the selection of these devices. However, conventional substrate mounted module packaging design does not take into account the requirements of pulsed power applications [6], [12].The required high voltage could be met by choosing single power MOSFET. But it requires special custom made solid state devices where special requirements are to be considered during the manufacturing the devices. The mass manufactured devices are limited due to limited withstand voltage levels and the isolation required between gate trigger circuit and power MOSFET. Recent advancements in semiconductor doping and deposition techniques have led to high-volume production of power MOSFETs capable of nanosecond-scale slew rate, of tens of ampere current ratings and Rds-on (drain-source on resistance) in the low ohms while still being capable of switching hundreds of volts [22-26]. Such devices allow for decreased circuit complexity due to their simple drive requirements, fast slew rate, and high power capacity.

This brings an alternate square wave pulse generator design by taking the series combination of power MOSFETs to generate the required voltage of affordable cost using mass manufactured devices. If one connects several devices in series and each device supports a share of the applied voltage, then the series string should be able to support more voltage than any single device could support alone. But, such series connections require an individual gate-to-source triggering voltage for each MOSFET device. Even though transformers with multiple secondaries reduce the independent triggering voltage to a single supply, they introduce time delay, the generator as bulky and economic penalties. A reliable method of stacking power MOSFETs, placing them in series, is proposed in this paper. The operation of this circuit is based on voltage division among the effective gate-source capacitance of the MOSFETs.

The triggering method for the HVPG is shown in detail in Figure 5. The drain of each device is connected to the source of its neighbor. The load may be resistive type or inductive type. In this paper, a resistive type load is assumed. All the MOSFETs gates are connected to a capacitor except the MOSFET which is nearest to the common ground. This lowest MOSFET gate is directly connected to the triggering source. This method of triggering is based on a model for gate charge transfer that is commonly accepted among many device manufacturers.

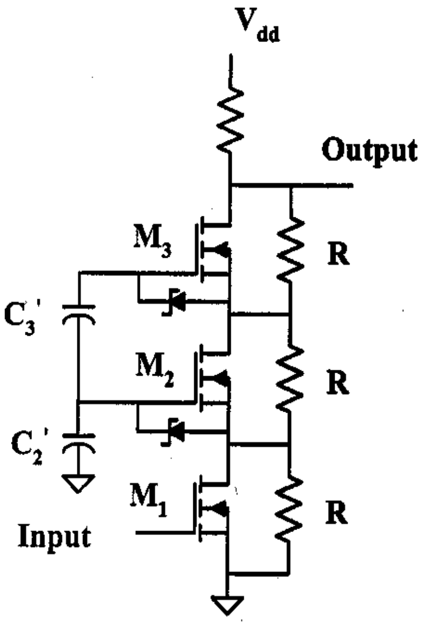

Fig. 5. Proposed gate triggering method for stacked power MOSFETs.

The DC drain-source voltages of the MOSFETs are equal prior to being triggered, i.e. $V_{DS1} = V_{Ds2} = V_{DS3}$ and the gate-source each MOSFET is 0V. When switching takes place the effective capacitance between the gate and source of each MOSFET is the effective gate source capacitance C_{gseff}. Initially the charge on C_2'

$$Q = C_2' \times V_{DS}' \tag{2}$$

After switching takes place, assuming 20V across the gate-source terminals, this charge is distributed between effective gate source capacitance and C_2', i.e.

$$Q = (20 \times C_2') + (20 \times V_{DS}') \tag{3}$$

Equations 2 and 3 may be combined and rewritten as

$$C_2' = \frac{20 \times C_{gseff}}{V_{DS}' - 20} \tag{4}$$

The $C_3^{'}$ is calculated in a similar manner except that a charge of $2\times V_{DS}^{'}\times C_3^{'}$ is stored on $C_3^{'}$. The value $C_3^{'}$ is given by
Equation 5 for V_{DS} » 20V.

$$C_3^{'}=\frac{20\times C_{gseff}}{2\times V_{DS}-20}\cong\frac{C_2^{'}}{2} \tag{5}$$

.

In general $C_n=\frac{1}{n-1}\times C_2^{'}$ for $n\geq 2$.

In the proposed circuit, IRF740, 400V, and 40A (pulsed current) MOSFETs are connected in series to generate 500 V square pulses and shown in Figure 6. Since the components in the circuits are non-ideal, it is advisable to leave a safety margin with respect to the maximum blocking voltage of the MOSFETs. Although there are four MOSFETs, this pulsed power supply still uses one driver circuit to drive four MOSFETs, which reduces the number of components and simplifies the board layout. The design of the series connection of the MOSFETs is based on extending the ideas that are presented in [27, 28] to high-voltage power MOSFETs. A resistive divider is added to stabilize the voltage rise at turn-off. Such a resistive divider is a common fixture when connecting semiconductor devices in series, whether thyristors, MOSFETs, or others. The other three MOSFETs are triggered based on a model for gate charge transfer that discussed above and is commonly accepted among many device manufacturers. This technique is based on voltage division among the MOSFETs that to be triggered.

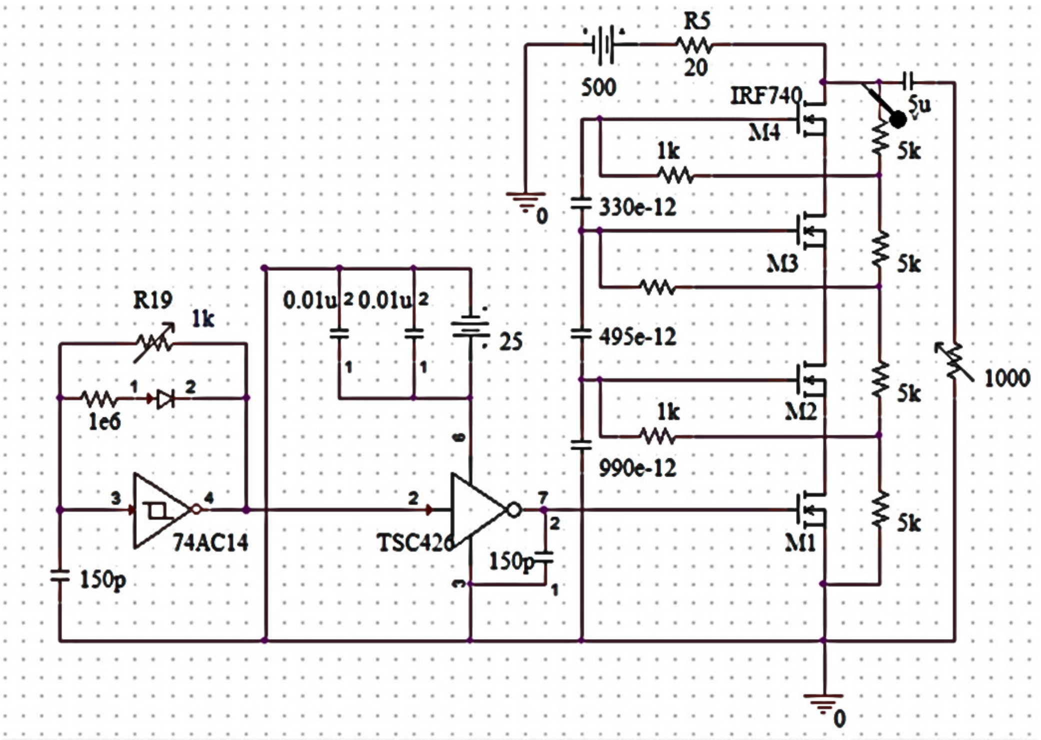

Figure 6. Stacked- MOSFET Circuit using IRF740

The lowest MOSFET's gate is triggered by TSC426 driver IC along with 74AC14 Schmitt trigger. The TSC426 translates TTL input to high voltage/current outputs. This produces the power MOSFET's minimum ON state resistance. These drivers rapidly charge and discharge the gate capacitance of even the largest power MOSFETs within millivolts of the supply rail. This particular version proved useful in that the low and high pulse widths could be made variable and the selection of the Semiconductor MC74AC14 integrated circuit was optimal from a performance standpoint. The MC74AC14 accepts standard CMOS Input signals and provide standard CMOS output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter–free output signals and have a greater noise margin. The designed circuit is suitable for varying the pulse width from few Nano-seconds to microseconds. This can be done by adjusting the triggering pulse width given to the lower MOSFET.

3. Simulation and Discussion

Using PSPICE, the system was simulated. Version 16.2 of the PSPICE software was used. This circuit was simulated and various aspects such as the effect of variation of load, and the effect of source resistance on the pulse parameters were studied. Certain capacitance and resistance values needed are changed to run it on PSPICE. The analysis is carried for different value of source resistance (R_S) and load resistance (R_L) to notify the importance of source resistance and load resistance. The source resistance value is very important for the selected application because it affects the output voltage magnitude and wave shape. The study on R_S is given in Figure 7 and Figure 8 for two different values of source resistances, 20Ω and 250Ω respectively. The wave shape is also an important factor to inactivate and improve the level of micro-organisms presented in food[30]. So it is required to retain the wave shape of the generated pulses to avoid the reversible electroporation. The food conductivity reaches its maximum value after subjected to initial consecutive pulses. It causes reduction in pulse magnitude and obviously slows down the inactivation process. It was observed from the simulation analysis that the minimum source resistance maintains the wave shape with acceptable voltage reduction.

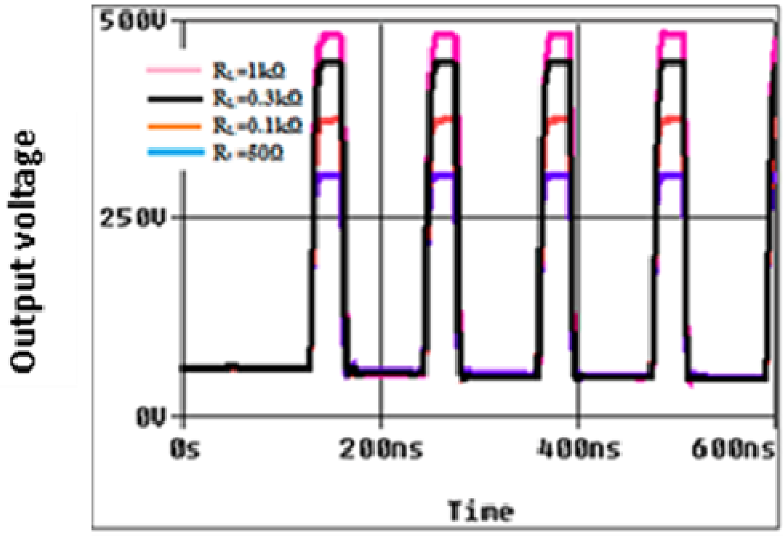

Figure 7. Output Pulse voltage variation if source resistor (R_5 in Figure 6) is 25 Ω

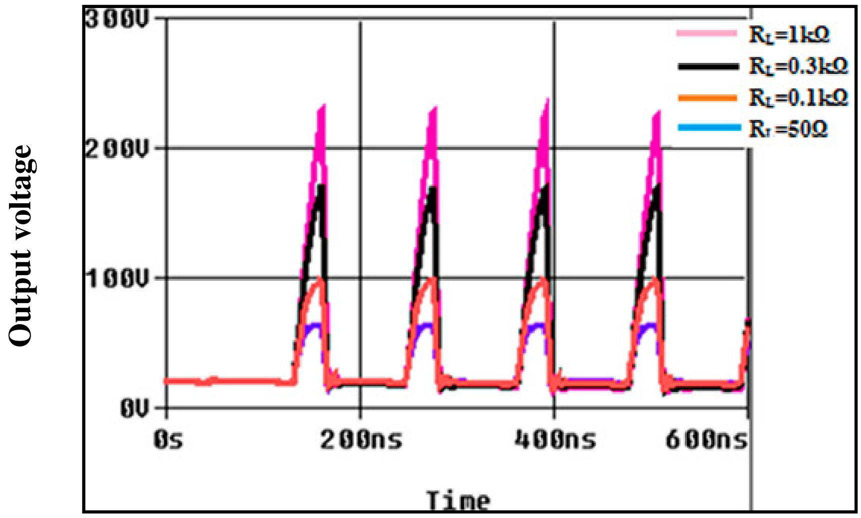

Figure 8. Output Pulse voltage variation if source resistor (R_5 in Figure 6) is 250 Ω

The energy efficiency also could be increased by minimizing the pulse width and increasing the pulse repetition rate for biological applications. The output pulse width can be varied by adjusting R_{19} and given in Table 1. It was observed that the pulse width can be changed from 38ns to 7 micro second without much change in fall time and rise time of the pulse. It was observed that the changes in pulse width and rise time are almost ignorable if the source resistance value in kept minimum. So the proposed circuit is suitable to vary the pulse width from 38ns to 7µs.

Table 1. Influence of Feedback resistor R_{19} on Pulse parameters

Value of resistance R_{19}(Ω)	Rise time (ns)	Fall time (ns)	Pulse width(ns)
500	134	5.35	38
700	187	4.92	51
1k	10	6.53	73
5k	11	7.70	369
20k	14	5.90	1430
50k	12	7.60	3540
75k	12	0.00	5330
100k	12	0.00	7120

The gate-source voltages are shown in Figure. 9.The voltages are within the 35V voltage limit. There is a transient overvoltage at turn-on, indicating that a zener diode for circuit protection may be appropriate. There is also a transient at turn-off, indicating that a zener diode and a fast diode in parallel with it from source to gate may be appropriate as well.

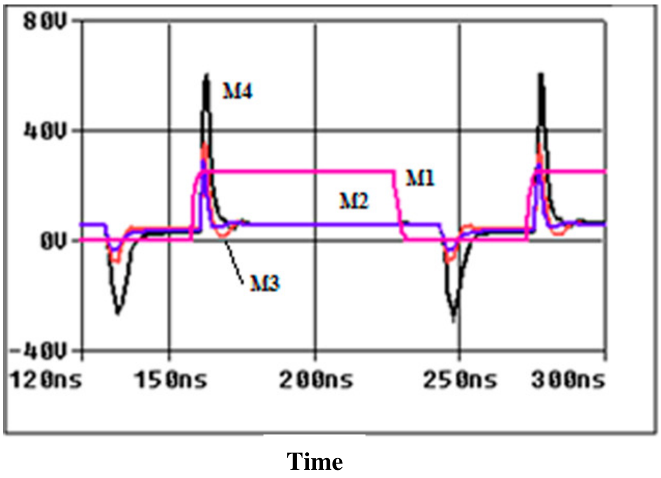

Figure 9. Gate-Source voltages of series connected MOSFETs (M1 –M4)

4. Implementation of Multi MOSFET circuit using IRF740

The MOSFET circuit was built and also tested at 500V. A series stack of IRF740 MOSFETs were connected as shown in Figure 5. The source resistance was designed as low as possible (R_s = 25Ω) to reduce the changes in wave shape which was analysed. The photograph of experimental setup is shown in Figure 10. The investigation of load resistance is comparable with those of the experimental results. The implemented circuit output is shown in Figure 11 and Figure 12 for source resistance value of 25Ω and 250Ω respectively. The waveform was recorded on a Agilent Technologies 6000, 100MHz, 2 GSa/s Digital Storage Scope.

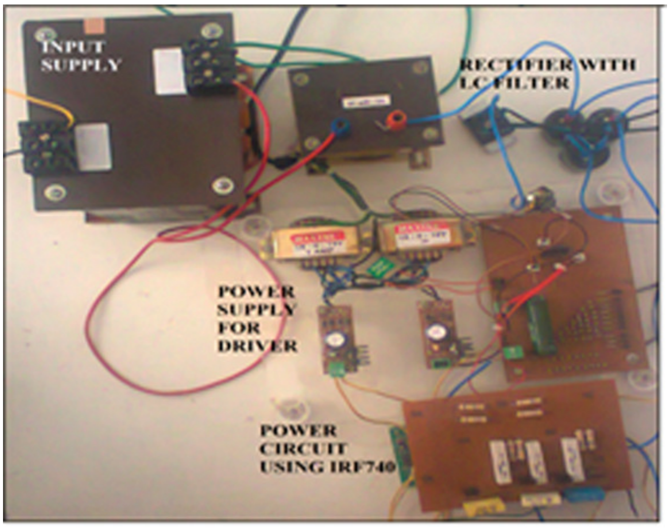

Figure 10. Experimental set up of Multi MOSFET design using IRF740

The experimental result shows the impact of source resistance on the output pulse. From experimental and simulation results, it appears that voltage balancing behaviour, static and dynamic, is superior to other conventional PEF methods. This method appears to be faster than other methods without expensive control hardware or software. Additional parts count is lower than other methods, particularly on the gate side, being less than a single small capacitor per switching device.

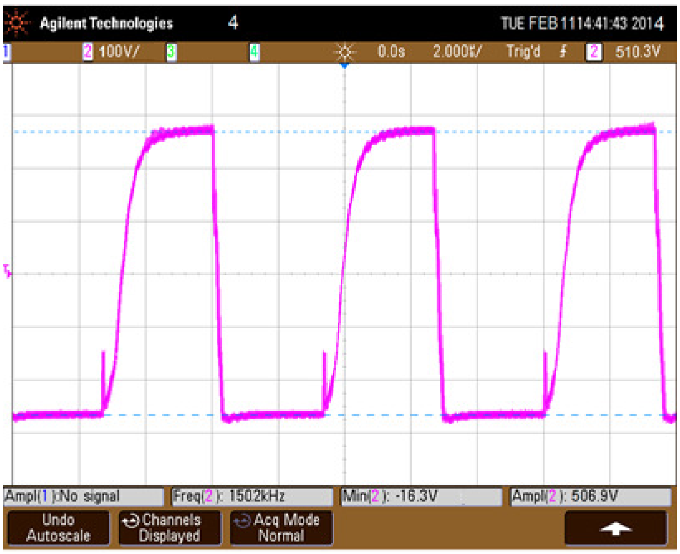

Figure 11. Experimental Output voltage waveform tested at 500V source resistance of 25Ω.

Figure 12. Experimental Output voltage waveform tested at 500V for source resistance of 250Ω

5. Conclusion

The proposed pulse generator was implemented and tested. A method to trigger MOSFETs and IGBTs without transformer coupling has been presented. The method is based on a voltage division across a series of capacitances. The device capacitance must also be considered while choosing series capacitance, most of which are internal device capacitances. The voltage stress is reduced in the Multi-MOSFET circuit by connecting devices in series. It improves the compactness and low setup cost. This method appears as faster than other methods and does not need any additional hardware or software. This method may be classed as a gate-side technique for voltage balancing. There is no expensive isolation transformer and, hence, no additional balancing regulators to compensate for delay caused by transformer coupling. The pulse width reduction maintains the processing temperature of PEF technology within the range and processing time also has been reduced by increasing the switching frequency. Thus the MOSFET based PEF generator may enhance the microbial inactivation level with less processing time. The proposed MOSFET PEF generator design is aimed to reduce the driver complexity and expensive less one for research purpose.

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