Integral screen printed solar cells panel

Y. Boukennous*, B. Benyahia, M.R. Charif, A. Elamrani and M.F. Moussa

Silicon Technology Unit; Solar Cells Laboratory,
2, Bd Frantz Fanon, B.P. 399, Alger-Gare; Algeria

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Abstract - *This paper summarizes our activities in the field of process technologies for the fabrication of photovoltaic devices. The study is strongly focused on the integral screen printing technique for the fabrication of single crystal solar cells, using standard equipments available in our laboratory. The challenging aim of this survey is to attain encouraging results with very modest means. Knowing that any problem coming unexpectedly with the cell structure may influence more than one electrical parameter and as the process consists on several steps; we will stop at each stage and discuss the factors, which affect it. In pursuit of this goal a doping phosphorus[1], a back contact silver-aluminium[2], a front side silver[3] and an anti reflective coating[4] commercial pastes are printed and fired. The 36 fully screen printed solar cells connected in series offer a module with power output of 31 Watts[5] and 11 % as efficiency.*

Résumé - *Cet article résume nos activités dans le domaine des procédés technologiques pour la fabrication des dispositifs photovoltaïques. L'étude est principalement orientée sur la technique intégrale d'impression d'écran pour la fabrication des cellules solaires monocristallines, en utilisant les équipements standard disponibles au laboratoire. Le principal objectif de ce papier est d'atteindre des résultats appréciables avec des moyens très modestes. En sachant que tout problème qui vient inopinément avec la structure de cellules, peut alors influencer plus d'un paramètre électrique et comme le procédé de fabrication se déroule en plusieurs étapes; nous nous arrêterons à chaque étape et nous discuterons sur les facteurs, qui l'affectent. Pour suivre le but assigné, un dopage en phosphore, un contact arrière en argent-aluminium, une partie avant en argent, et des pâtes commerciales pour une couche anti réfléchissante sont imprimés et sont mis dans un four. Les 36 cellules solaires imprimées sur écran et connectées en série donnent un module photovoltaïque d'une puissance de 31 watts et un rendement de 11 %.*

Keywords: Single silicon - Screen-printing - Temperature-time.

1. INTRODUCTION

The integral screen printing technology reduces the cell fabrication time, the steps and the thermo-electric energy with respect to conventional methods. Therefore, the technique offers the advantage of low cost solar cell production, which is sought by the photovoltaic panel manufacturers.

The realization of fully screen printed solar cells has been outlined in many papers [1-4]. The problem with this technique resides in a good knowledge of the physicochemical properties of the inks. In fact, if a paste gives good results on a definite process it is not obvious to apply it comfortably on another process. Things change drastically from one paste to the other and the optimisation of the electrical parameters of the cell has to be repeated for each ink. The recommended supplier's profiles are given as an indication and one has to take them as a starting point. Moreover, optimising each step taking into account the others is primordial to gain appreciate efficiency, because if one of them deviates, the final device will suffer. Therefore, the result will depend on the starting material, capabilities of the equipments and user's processing parameters such as screen design, printing and firing. Nevertheless, one can still come to closer results after thorough investigating.

* Boukennous_y@yahoo.fr

To start with the technique, we adjusted the printing variables in order to get optimal deposit layers, depending on the application, by combining stainless steel wire cloth, emulsion thickness coating screen, mechanical printing parameters and rheological properties of the pastes. The equipments used for are: a semi automatic screen printer DEK 1760 RS, a belt dryer DEK 1209 and a heated resistance belt furnace BTU 7354 M.

2. TECHNOLOGY

The study was carried out on as-cut p-doped single crystal silicon wafers, 4 inch in diameter, 0.5 to 2.5 Ω-cm resistivity, <100> oriented and about 450 μm thick. The process achieved is classic and involves the following steps:

2.1 Chemical preparation and texturization

To remove dust, roughness and damage from the as cut silicon wafers, an aqueous bath of NaOH is used. Then the shiny wafers were textured in an adequate NaOH-Alcohol solution to roughen the surface in order to decrease the optical reflection of the wafers.

Many experiences were performed and showed that poor texturing is due essentially to non-optimised etching temperature-time, and/or NaOH concentration, and/or impurities in the bath. Consequently, maximum care must be observed with these parameters and with continuous agitation for succeeding on the operation.

Figure 1 shows the state of surface of a random sample taken from a batch of 25 wafers treated in one go. We can see that the surface is uniformly textured and the pyramids are regular enough.

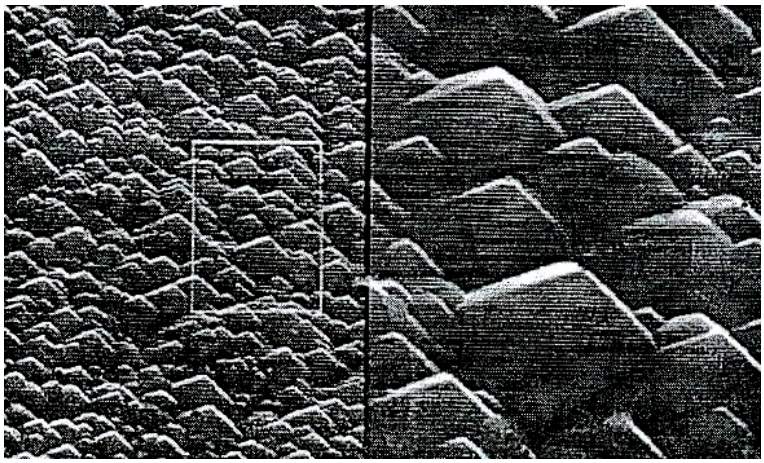

Fig. 1: Surface covered with microscopic pyramids observed by MEB

2.2 Emitter diffusion

A phosphorus-doped paste is printed through screens with mesh sizes of 150 to 400. The thickness of the deposited layer is uniform, covering perfectly the textured surfaces. Phosphorous atoms diffuse into the silicon to a controlled concentration and depth on the front side of the wafers depending on the screens, the screen printer set up and the relation temperature-time. This advantage of the technique dispenses us from the step of elimination of the junction on the back as in the case of a gaseous diffusion.

The printed wafers are dried for 10 minutes at 150 °C then followed by a firing. We have prepared several emitters varying the temperature profile from 910 °C to 960 °C at constant time. Then, the glassy oxide was removed by immersion in a solution of hydrofluoric acid.

To characterize the achieved emitters, we used the electronic microscope (MEB) for the junction depth and the four probes for the sheet resistivity. The MEB revealed homogeneous junctions, as illustrated in figure 2, while the four probes showed a wide range of sheet resistivity values, represented in figure 3.

From figure 2 we can see, after cleaving the sample (on the top) and staining (on the bottom), that the junction follows perfectly the shape of pyramids and could be comfortably measured.

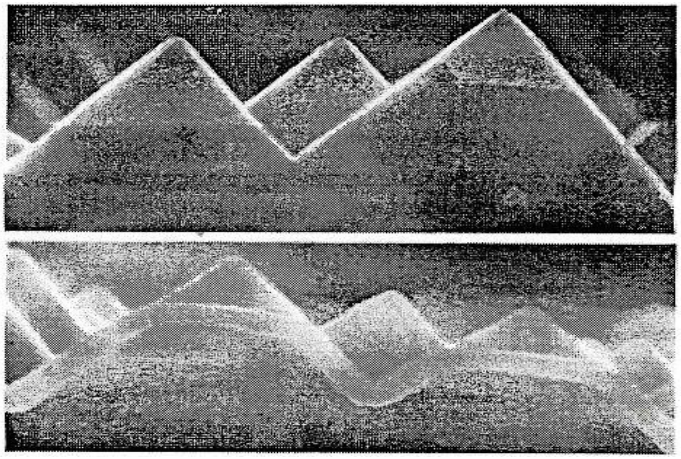

Fig. 2: Junction observed by MEB

As seen in figure 3, the results are in agreement with those given in the literature. The curves are useful for direct reading of the sheet resistance and the junction depth. At constant drive-in time, the sheet resistance falls with temperature whereas the junction depth of the processed emitters grows.

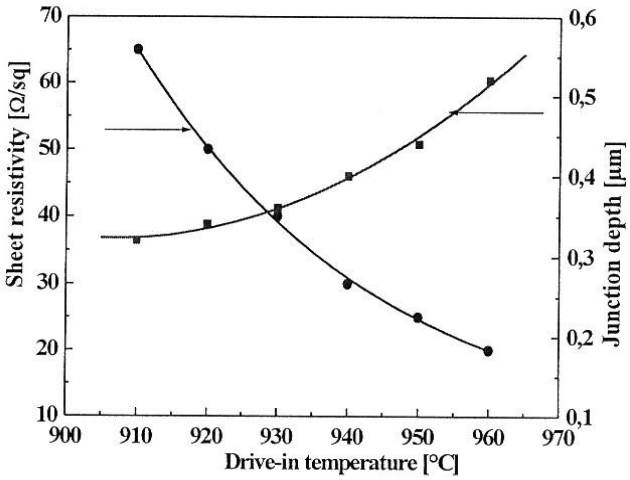

Fig. 3: Sheet resistivity (▪) and junction depth (•) versus drive-in temperature

Phosphorus diffusion profiles were measured by the anodic oxidation technique in order to get the surface concentrations of dopants. The concentration profile is determined by differential resistivity measurements while a thin layer is removed repeatedly by anodic striping. The data

measured are converted into an impurity using Irvin's resistivity-impurity concentration. The typical results obtained for the profiles firing cited above are illustrated in Table 1.

Relatively high surface concentration (C_s) with respect to classic emitters is needed to obtain good ohmic contact while sintering the front metallization. From Table 1, we can see that the higher the temperature is, the higher the C_s is, which is favourable to screen printed contacts.

Table l: Surface concentration (C_s) vs diffusion temperature using Irvin's curves

T_p (°C)	X_j (μm)	C_s (10^{20} at/cm^{-3})
910	0.32	1.48
920	0.34	1.75
930	0.36	2.06
940	0.40	2.42
950	0.44	2.59
960	0.52	2.78

2.3 Edge isolation

To separate the front surface from the one at the back, a dry etching in CF4 plasma is achieved. The wafers are fixed in a coin stack and where approximately 1 to 2 um of the material were removed on the edges of the wafers (ring etching).

Many problems such as non-uniform thickness and size of the wafers, loose coin stack, non-optimised time etching and poor plasma distribution could occur, resulting in losses.

The plasma etcher[6] used is well controlled and maximum attention was taken with the dimensions of the wafers, so this operation was successfully performed.

2.4 Back metallization

We opted for a silver/aluminium alloy, which provided a double advantage. The first one is the role mat plays the aluminium for the excellent ohmic contact. The second is the possibility to solder easily the interconnecting leads on rear contact for regrouping the cells without overprinting another solderable metal layer [5, 6].

The paste composed of 70 % silver and 2 % aluminium, could not create the back surface field (BSF) due to the low aluminium rate containing. Back metallization must have low sheet resistivity and contact résistance as well as strong adherence. The wafers were processed at different temperatures ranging from 600 to 800 °C at constant time. The results showed that if the temperature-time profile is too low, the aluminium did not alloy and then pulled off. To the opposite, if the temperature-time profile is too high, the aluminium diffused too far and oxidized. Moreover, in this case the impurities contained in the ink could contaminate the device.

Rich of all these informations, we restricted the temperature in the range 680 – 720°C. After many investigations, 700°C has been found to be generally optimum with appreciable open voltage.

2.5 Front metallization

The front contact grid is the most difficult step to attain and control. The first obstacle implies the realization of a grid pattern with narrow but deep fingers to allow enough light reaching the active region, while giving acceptable series resistance. The second one requires optimization of the temperature-time. To succeed on the first operation, maximum precautions should be taken with the viscosity of the paste. In fact, if the viscosity is not properly adjusted, narrow lines will widen resulting in an increase of the metal reflection.

The second constraint is to achieve optimum temperature-time profile for strong adherence, low contact resistance, and minimum reflectance, without fatal effect on the emitter. For the

junctions obtained in the order of 0.2 to 0.8 μm and the ink available, it is quite clear that it was necessary to test several firing cycles. This is essentially owed to the chemical composition of the paste (glass frit rate) and more than that to the contact metal-semiconductor [7-9].

Therefore, rather, than to proceed to a additional selective diffusion under the gridlines to improve ohmic contact, we used a lightly phosphorous doped silver paste. The achieved samples fired in the range 600-800 °C indicated that lower temperature-time firing resulted in poor adhesion resulting in high contact resistance; otherwise, higher temperature-time oxidized the silver and sometimes damaged the emitter. At the last, the junction of 0.4 μm deep at 750 °C fast fired offered the best results.

2.6 Anti-refection coating

The anti-reflective coating (ARC) is printed after metallization to prevent the losses by reflection. The properties of the TiO_2 are controlled by varying the firing and deposition conditions. A study in this respect showing preliminary results had already been published the authors [10].

Unfortunately, screen printed ARC on textured surfaces did not offer any improvement. On the contrary, it degraded the device. To avoid this contrariety, we repeated the process on untextured substrates. The cells were processed in as similar a manner as possible for the comparison. Then, we compared those untextured but AR coated with those uncoated textured ones. The results showed a finite advantage for the latest. Therefore, due this result, we eliminated this step from the processed panel. Knowing that the ARC, while printed before metallization, could improve the contact resistance and protect the wafers from impurity diffusion, we are still aiming at improving the technique of its deposition on textured samples using the means available in our laboratory.

2.7 Package construction

Our long experience in solar photovoltaic module encapsulation allows us to do the good choice for the packaging technique and material. The material selected must have high transparency to solar insolation to reach the cells and great protection against weather inclemency. The fabrication procedure as developed in our factory is shown in figure 4. The operation is well understood and does not present any particular problem.

An exploded view detailing all components for the encapsulation is given below (Fig. 4).

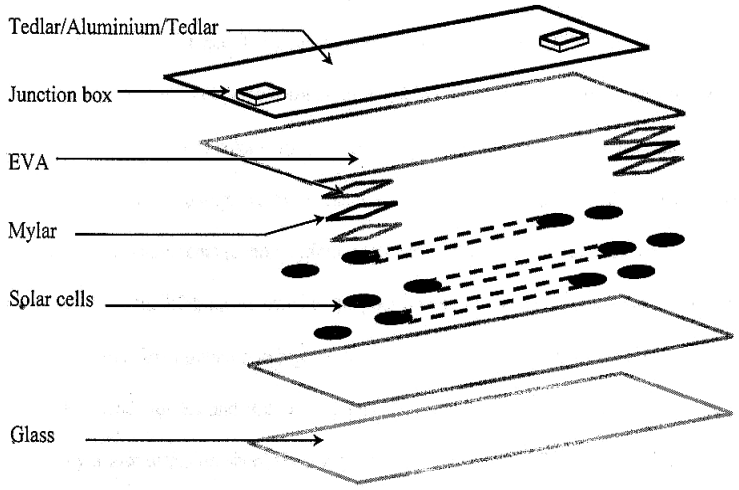

Fig. 4: Exploded view for module fabrication

3. DISCUSSION AND CONCLUSION

As illustrated the I-V characteristic shows a relatively weak short-circuit current (I_{sc}) and open-circuit voltage (V_{oc}). It also point out the effect of both the series resistances (R_s) and a little more the shunt resistance (R_{sh}), resulting in moderate fill factor (FF).

As well known, I_{sc} and V_{oc} have a common restrictive factor, which is the minority carrier lifetime. For high efficiency solar cells, electron lifetime should be around 10 μs or more.

Suspecting the wafers quality, we have characterized the samples using μ-PCD[7] technique. The results of measurements (average lifetime) values performed on 5 samples are in 2 - 8 μs. The low values of the lifetime are owed to the poor quality of the starting material. Priori, this may be one of our first limitation in high performances. A study on this respect is going on.

On the other hand, for R_s and R_{sh}, technological processing is incriminated. In fact, R_s is increased by a low diffusion sheet resistivity and/or poor sintered silver or silver-aluminium and/or non-optimised design and print gridlines pattern. Whereas, R_{sh} is principally affected by incomplete edge etch and/or broken pyramids which could be eventually covered by metal and/or impurities presence during high temperature firing such as diffusion or metallization.

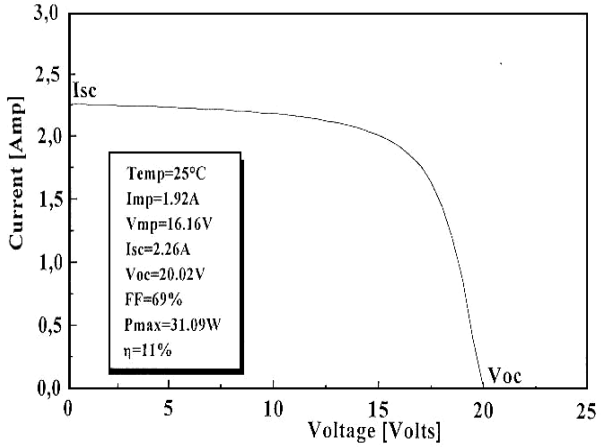

Fig. 5: I – V characteristic of the performed panel

We have controlled the surface and shape of the pyramids and found that they were correct. The bath used for etching and texturing was prepared and executed in a clean room, this suppose that the wafers were clean when presented to the diffusion step.

The visual inspection showed that the fingers were narrow enough and thick without interruption.

Free of all these problems, for the done process, we suspect that during firing the fumes were not effectively removed. They could have been deposited on the front side of the wafers resulting in a reduced optical absorption of the solar cells.

In our mind, another problem could be the possible contamination by the contingency of impurities presence in the belt furnace used daily by others with different sources and metals.

As a conclusion, we say that the moderate results are closely imputed to the quality of the starting substrates and capabilities of the processing equipments available. Nevertheless, this survey allowed us to demonstrate the feasibility of photovoltaic cell realization by the screen printing technique using conventional equipments.

Our future work will consist in improving this technique. To obtain this goal, the study will be based along these 3 mains lines:

- Testing all the process on a different type of the starting wafers;
- Deposition of the ARC before metallization to reach a better ohmic contact while sintering the front metallization. This will protect the wafers against metallic impurities diffusion out of the furnace and pastes;
- Co-firing the front and rear contacts to simplify the process for optimum quality-cost.

This will also prevent from breakage and rough handling which are often sources of contamination.

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[1] Phosphorus paste: Soltech P101
[2] Back contact silver-aluminium: Ferro 3398 Ag-Al
[3] Front side silver: Ferro 3349 Ag
[4] Anti reflective coating: Ferro DP 99-007
[5] Measured under standard conditions: SPI-SUN 240 Simulator
[6] Plasma etcher: Plasma Technology SE 80
[7] μ-PCD: SEMILAB (Hungary)