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Study of the performance of ballistic carbone nanotube FETs

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Abstract
Using a two-dimensional (2-D) simulation, we study the impact of varying the nanotube diameter and gate oxide thickness on the performance of a ballistic nanoscale carbon nanotube field effect transistor (CNTFET). Our results show that the nanotube diameter influences the I_{ON}/I_{OFF} current ratio; the drain induced barrier lowering (DIBL), the subthreshold slop as well as transconductance and drain conductance. We also show that these device characteristics are affected by the gate oxide thickness. Thus, nanotube diameter and gate oxide thickness must be carefully taken into account when designing robust logic circuits based on CNTFETs with potentially high parameter variability.
Keywords: *Carbon nanotube; Field- effect transistor; Ballistic; Carbon nanotube diameter; Gate oxide thickness.*

1. Introduction

Since the first reports of single-walled carbon nanotubes (CNTs) in 1993 [1, 2], they have been the subject of intense interest for basic and applied research. In particular, single-walled carbon nanotube (SWCNT) field-effect transistor (CNTFET) is considered as one of the most promising candidates for enhancing functionality of silicon based complementary metal-oxide-semiconductor (CMOS) circuits and extending Moore's Law [3-6].
Due to the small diameter, thin high-k gate insulator, and a good S/D metal contact, the CNTFET demonstrates the best performance to date. Recently, CNTFETs have been fabricated successfully [7–9]. It has been reported that they have shown better performance than present silicon transistors with the equivalent sizes. They are particularly attractive for high-speed applications due to their quasi-ballistic properties and high Fermi velocity (10^6 m/s) [10-11]. Rapid progress in the field has recently made it possible to fabricate digital and analogue CNTFET-bases circuits, such as logic gate, static memory cells and ring oscillators [12, 13].
In this paper, we will discuss the role of nanotube diameter and gate dielectric thickness on the performance of CNTFETs over wide range by reference to I_{ON}/I_{OFF} current ratio, subthreshold slope, the drain induced barrier lowering (DIBL) as well as transconductance and drain conductance using a two-dimensional (2-D) simulation. Because to explore the role of CNTFETs in future integrated circuits, it is important to evaluate their performance and the nanotube diameter and gate dielectric thickness have direct relevance for the electrostatic control in a CNTFET.

2. Simulated device

The modeled device, a coaxially gate, n-type CNTFET is schematically shown in figures 1(a) and 1(b). The nanotube length is 50 nm, consisting of ~1.2×10^4 carbon atoms. The intrinsic channel length is 20 nm, and the doped source/drain length is 15 nm.
To simulate the behavior of a CNTFET, the following model is used at different nanotube diameters and gate oxide thicknesses. The chiralities of the CNTs used are (13,0), (16,0), (19,0), (23,0), (25,0). In addition the gate oxide thicknesses (tox) used are 1.5 nm, 3 nm, 4.5 nm, 6 nm and 7 nm. The high-k gate dielectric is fixed at k=16, correspond to the dielectric constant reported for HfO_2.
For our simulations, we assume that the metal-nanotube contact resistance, R_c = 0, and carrier transport through nanotube is ballistic (no scattering). No gate-to-source or gate-to-drain overlap is assumed. The applied drain (V_{DS}) and gate (V_{GS}) biases vary from 0 V to 1. All calculations have been done at room temperature (T = 300 K).

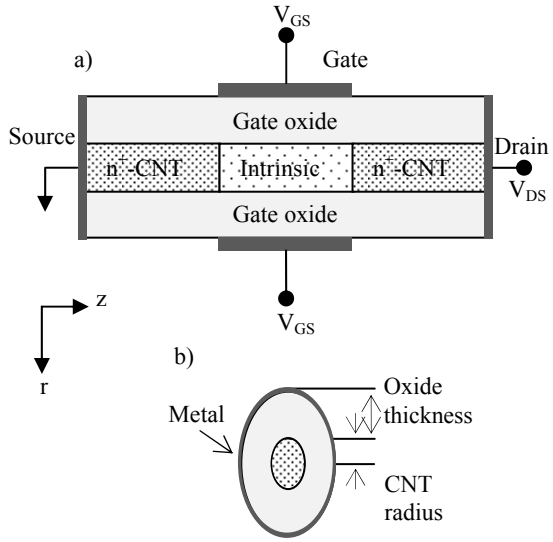

Figure 1. Schematic diagrams of the modeled, coaxially CNTFET.

3. Model:

Many models have been proposed for simulating the characteristics of CNFETs [14,15]. The specific model chosen for this study is based on capacitance model [15], as shown in Fig. 2.
The circuit diagram in Fig. 2 shows the simple model that represents the potential at the top of the barrier when taking into account the effect of the three terminals (source, drain, and gate).

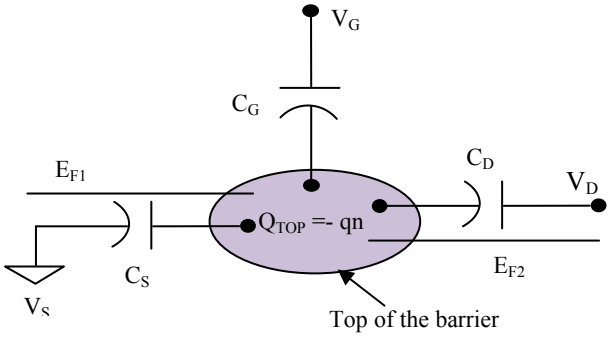

Figure 2. Two dimensional circuit model for ballistic transistors.

The mobile charge is represented by the shaded region in Fig. 2 and is determined by the combination of the local density of states at the top of the barrier, the location of the source and drain Fermi levels, E_{F1} and E_{F2}, and by the self-consistent potential at the top of the barrier, Uscf.

When the terminal biases are zero, the equilibrium electron density at the top of the barrier is:

$$n_0 = \int_{-\infty}^{+\infty} D(E) f(E - E_F)\, dE \qquad (1)$$

Where D(E) is the local density of states at the top of the barrier, and f(E-E_F) is the equilibrium Fermi function. When a bias is applied to the gate and drain terminals the self-consistent potential at the top of the barrier becomes Uscf, and the states at the top of the barrier are now populated by two different Fermi levels. The positive velocity states are filled by the source, according to:

$$n_{1=} \frac{1}{2} \int_{-\infty}^{+\infty} D\big(E - U_{scf}\big) f(E - E_{F1})\, dE \qquad (2a)$$

and the negative velocity states are filled by the drain according to:

$$n_{2=} \frac{1}{2} \int_{-\infty}^{+\infty} D\big(E - U_{scf}\big) f(E - E_{F2}) dE \qquad (2b)$$

Where, E_{F1}= E_F, and E_{F2}= E_F – qV_{DS} [2]. A change of variables can be used to re-express these equations as:

$$n_{1=} \frac{1}{2} \int_{-\infty}^{+\infty} D(E) f_1(E) dE \qquad (3a)$$

$$n_2 = \frac{1}{2} \int_{-\infty}^{+\infty} D(E) f_2(E) dE \qquad (3b)$$

Where

$$f_1(E) \equiv f\big(E + U_{scf} - E_{F1}\big) \qquad (4a)$$

and

$$f_2(E) \equiv f\big(E + U_{scf} - E_{F2}\big) \qquad (4b)$$

With eq. (3), the total electron density at the top of the barrier is $n = n_1 + n_2$, and can be determined if the arbitrary density of states, *D(E)*, the source and drain Fermi levels, and the self-consistent potential, Uscf, are known.
The self-consistent potential is determined by solving the two-dimensional Poisson equation as represented by the 2D model in Fig. 2 with the common terminal evaluated at the bias induced charge, $\Delta n = (n_1 + n_2) - n_0$. Ignoring mobile charge in the channel, the Laplace potential at the top of the barrier is then:

$$U_L = -q(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S) \qquad (5)$$

In this equation (5), the three α's describe how the gate, drain, and source control the Laplace solution [2] and are given by:

$$\alpha_G = \frac{C_G}{C_T} \quad \alpha_D = \frac{C_D}{C_T} \quad \alpha_S = \frac{C_S}{C_T} \qquad (6)$$

Where C_T is defined as the parallel combination of the three capacitors in Fig. 2.
For an optimally constructed MOSFET, the gate controls the potential in the channel which means that $\alpha_G \approx 1$ and, α_S, $\alpha_D \approx 0$. The model is completed by taking into account the effect on the potential at the top of the barrier due to mobile charge with:

$$U_P = \frac{q^2}{C_T} \Delta n \qquad (7)$$

Therefore, U_{scf} is equal to:

$$U_{scf} = U_L + U_P = -q(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S) + \frac{q^2}{C_T} \Delta n \qquad (8)$$

Equations (2) and (8) represent two coupled nonlinear equations for the two unknowns n and U_{scf}. These equations can be solved iteratively to find the carrier density and self-consistent potential at the top of the barrier. Finally, the drain current is evaluated from:

$$I_D = \int_{-\infty}^{+\infty} J\big(E - U_{scf}\big)[f(E - E_{F1}) - f(E - E_{F2})] dE \qquad (9a)$$

Where J(E-Uscf) is the "current-density-of-states", which is expressed as:

$$J\big(E - U_{scf}\big) = \frac{1}{2} q \left(\frac{2}{\pi} \sqrt{\frac{2(E - U_{scf})}{m^*}} \right) D\big(E - U_{scf}\big) \qquad (9b)$$

4. Results and discussion:

4.1. Investigation of effect of nanotube diameter:

In this section, the gate oxide thickness is fixed at 1.5nm and high-k gate dielectric is fixed at k=16, while the nanotube diameter (d) is varied. Figure 3 presents the I_{ON}/I_{OFF}

current ratio as a function of the nanotube diameter. I_{ON} is obtained at V_{GS} = 1 V and V_{DS} = 1 V, I_{OFF} is defined as the current obtained for V_{GS} = 0 V and V_{DS} = 1 V. It can be observed that I_{ON}/I_{OFF} ratio is improved with increase in the nanotube diameter. This comes from the correlation of the band-structure with the CNT diameter. Using a larger diameter reduces the bandgap, therefore both the ON-current and the leakage current I_{OFF} increase, and I_{ON} increases rapidly. Thus a significant increase of the I_{ON}/I_{OFF} ration is observed when the nanaotube diameter is increases. So this point must be carefully taken into account to obtain the best electrical characteristics in perspective to build reliable logic circuits based on CNTFETs.

For short channel devices, application of a high drain-to-source bias can shorten the threshold voltage and increase the off-currents. This is known as drain induced barrier lowering (DIBL). In CNTFETs, the DIBL effect is still a primitive problem and open for further study [16].

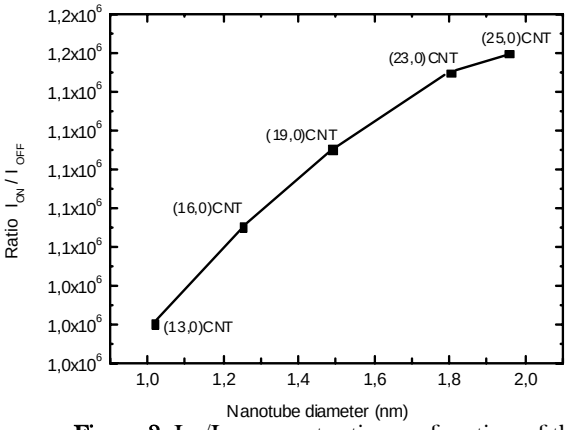

Figure 3. I_{ON}/I_{OFF} current ratio as a function of the nanotube diameter

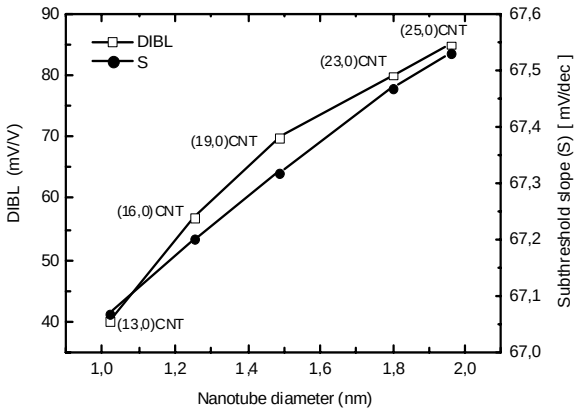

Figure 4. Drain induced barrier lowering (DIBL) and subthreshold slop versus nanotube diameter.

Figure 4 shows the effect of varying the nanotube diameter on the DIBL. The DIBL is accessed using the classical expression [17].

$$\mathrm{DIBL} = \frac{V_{TH}(\mathrm{Low}\ V_{DS}) - V_{TH}(\mathrm{High}\ V_{DS})}{\mathrm{High}\ V_{DS} - \mathrm{Low}\ V_{DS}} \qquad (10)$$

From the simulation results, it can be drawn that the DIBL is considerably improved with decreasing d; therefore, the control of gate on the channel becomes stronger. One notes a reduction around 53% of DIBL when CNT chiralities varying from (13, 0) CNT to (25, 0) CNT.

Another important parameter characterizing the short channel performance is the subthreshold slope (S). A small subthreshold slope is desired for low threshold voltage and low-power operation for FETs scaled down to small sizen. Figure 4 represents the evolution of subthreshold slope as a function of the nanotube diameter (d) for V_{DS} = 1 V. It can be observed that when the nanotube diameter decreases, S decreases slightly (practically remains constant around 67 mV/decade).

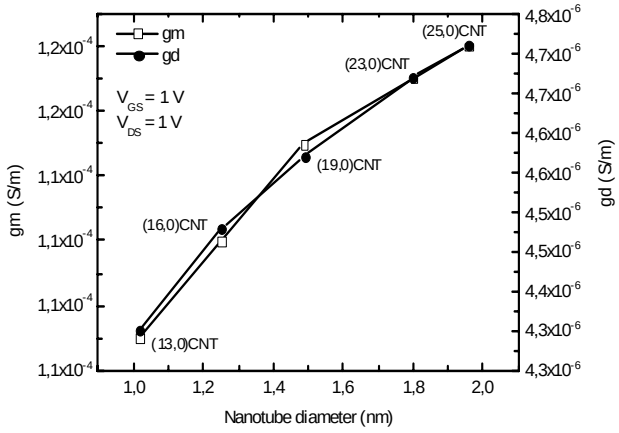

Figure 5. Variation of g_m and g_d at V_{DS}=1 V and V_{GS}=1 V as a function of nanotube diameter.

The transconductance, an important device parameter, is defined as measure of device gain and is directly related to the circuit speed. The transconductance gm curve is obtained by differentiating the drain current I_{DS} with respect to the gate voltage V_{GS} at a given drain bias $g_m=\partial I_{DS}/\partial V_{GS}$ [18]. As can be seen from Fig. 5, when the nanotube diameter increases the transconductance gm, increases. The drain conductance defined by $g_d=\partial I_{DS}/\partial V_{DS}$. Figure 5 also shows the variation of drain conductance gd, in saturation, for different values of d in a CNTFET. It is observed that gd is higher for larger d. One notes a voltage gain gm/gd around ~25 whatever the value of nanotube diameter d is.

4.2 Investigation of effect of gate dielectric thickness:

The I_{ON}/I_{OFF} current ratio of the CNTFETs with gate oxide thickness (t_{ox}) varying from 1,5 nm to 7nm are compared in Figure 6. I_{ON} is measured at V_{DS}= 1V and V_{GS}=1V, I_{OFF} defined as the current obtained for V_{DS} =1V and V_{GS}=0V.

It can be seen from the figure that with decreasing of t_{ox}, the I_{ON}/I_{OFF} ratio increases and lead to a high on- state current. This is associated with superior control of the gate voltage over the channel, which helps in reducing the off- state current.

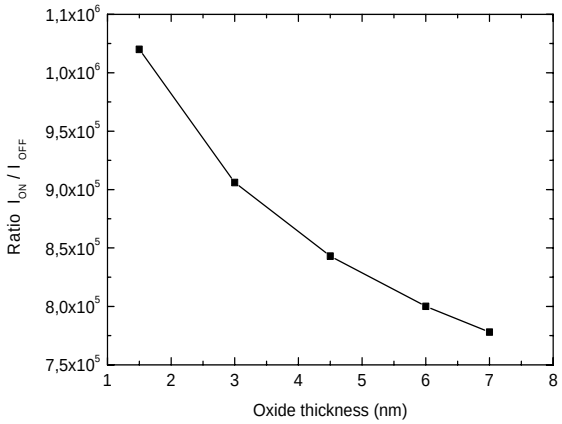

Figure 6. I_{ON}/I_{OFF} current ratio as a function of the oxide thickness

As can be seen from Figure 7 when t_{ox} decreases, the DIBL decreases. It is evident that the DIBL of device improves with decrease in t_{ox}. There for the control of gate on the channel becomes stronger.
Subthreshold slope is an important factor that increases the standby power dissipation in CMOS circuits.

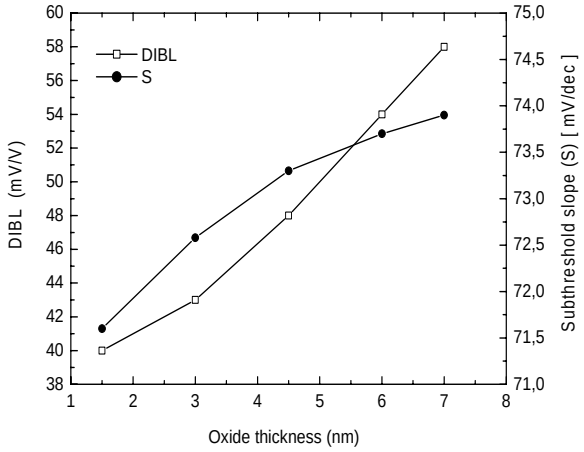

Figure 7. Drain induced barrier lowering (DIBL) and subthreshold slop versus oxide thickness.

A small subthreshold slope (S) is also desired for low threshold voltage for FETs scaled down to small size [19]. The lowest theoretical limit for S is: $S= (K_BT/q)\ln(10) \cong 60$ mV/decade at room temperature.

Figure 7 shows that the subthreshold swing decreases with decreasing (t_{ox}).

As shown in Figure 8, it is seen that as gate dielectric thickness (t_{ox}) increases the drain conductance, gd, and transconductance gm, continues to decrease.

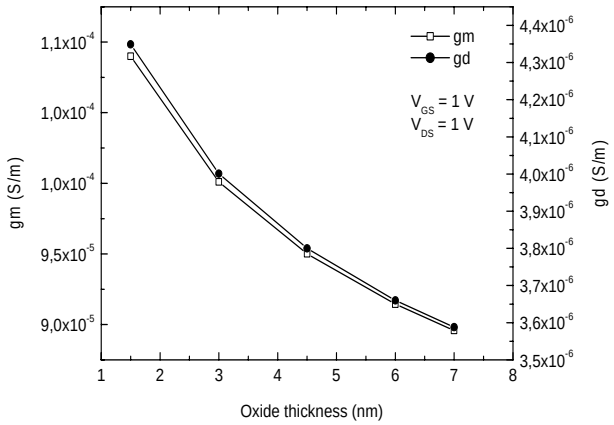

Figure 8. Variation of g_m and g_d at V_{DS}=1 V and V_{GS}=1 V as a function of oxide thickness

5. Conclusion

We implement a two- dimensional model to explore the behavior of a CNTFET at different nanotube diameters and gate oxide thickness.
Based on the I_{ON}/I_{OFF} current ratio, drain –induced barrier lowering (DIBL), subthreshold slope, transconductance and out conductance variation with different carbon nanotube (CNT) diameters and gate oxide thickness, the CNTFET behavior is evaluated.
We concluded that using large CNT diameter and thinner gate oxide are caused by the enhancement in on-state current, transconductance and out conductance. In addition, off-state current, DIBL and subthreshold slope improve in CNTFETs with thinner gate oxide, but they become worse in CNTFETs with large nanotube diameter.

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