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3D Numerical simulation of a dual metal (Aluminum, Titanium) horizontal square surrounding gate MOSFET

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Abstract

Essentially due to the uninterrupted scaling of MOSFET transistors, it has become absolute obligatory to explore for new transistors architectures in order to reach better control of short channel effects. Also the integrity and issues related to electrostatic performance associated with scaling Silicon MOSFET bulk sub 10 nm channel length promotes research in new device architectures such as SOI, double gate and gate all around GAA MOSFETs [1]. In literature GAA structure has been proposed to reduce the SCEs due to scaling of the MOSFET transistor. GAA structures, that are actually strong candidates for the next generation nanoscale devices, show an even stronger control of short channel effects.

In this paper, a double metal square surrounding gate MOSFET for reduces short channel effects is presented. Our results take into account quantum confinement. In the latter part of the paper some 2D simulation results of our structure has been shown using SILVACO TCAD tools. We will also exhibit some simulation results we obtained relating to the influence of some parameters variation on our structure), that have a direct impact on their threshold voltage and drain current. In addition, our Transistor showed reasonable Ion/Ioff ratio of (10^4) and low drain induced barrier lowering (DIBL) of 39mV/V

keywords: GAA ; SILVACO-TCAD ; quantum effects ; MOSFETs; dual metal.

1. Introduction

During the last decade, Field-Effect transistors have legitimate chipmakers to shrink these devices to only tens of nanometres in length designing new MOSFETs architectures. Indeed, as transistors become smaller, physical limitations of current planar transistors appears. MUGFET Si-based devices such as gate-all around (GAA) MOSFETs seem to be are very promising candidates for aggressively scaled CMOS, and can potentially solve various problems with scaling down the size of transistors . These problems include the electron tunneling due to thinner layers of the insulating barriers, the increased threshold leakage that comes with shorter channel length, and the corner effects produced by smaller sized and square corners. GAA transistors presented in this study own an excellent electrostatics, low power consumption, immunity to short channel effects that plays important role in devices, drain induced barrier lowering, handling out of the gate, and the reduction of leakage current [2],[3].

However beyond the 10 nm range, quantum confinement must be considered. These effects have been included in several books related to the square GAA JLFETs [4] [5], but none of quantum effects has been modeled in extremely devices - scale ,where quantum confinement effects become important and governing the performance of the device. The GAA MOSFET, which is basically a 3-D structure, cannot be analyzes directly the same way. One possibility is to solve Laplace's equation in rectangular coordinates by means of a series expansion in Bessel functions [6] and then Bohm quantum potential (BQP) model used in simulations allows to calculate a position dependent potential energy term using an auxiliary equation derived from the Bohm interpretation of quantum mechanics. This extra concentration is integrated in the whole structure and then this quantity is derived as C=dQ/dV [7].

In this paper, 3D quantum numerical simulation a double metal square surrounding gate MOSFET, that is a quadruple gate with square section , have been validated using SILVACO TCAD simulations in order to present some interesting characteristics and the influence of some parameters variation on our

structure, that having a direct impact on their drain current [8],[9].The threshold voltage is analyzed for device parameters such as gate length ratios, oxide thickness, silicon thickness, and doping concentration.

2. Device design

Our 3D device has been generated using SILVACO TCAD tools and is shown in figure1. The different parameters of our structure are assumed as follows: Gate Length of 9 nm, a lightly doped channel region 1.0E+17/cm^{3} (Boron) so that there is substantially no degradation of mobility due to channel doping, heavily doped drain and source regions (Arsenic) 1E20cm^{-3}, silicon dioxide with 1 nm thickness used as gate oxide allows to stop the gate tunneling current, dual metal gate aluminum are considered with φM1 = 4.1 eV for aluminum and φM1 = 4.4 eV for Titanium , the height and width of our device are W=H=5nm. As shown in Figure 1 our Gate-all-around FETs square looks like FinFETs excluding that the gate material surrounds the channel region on all sides.

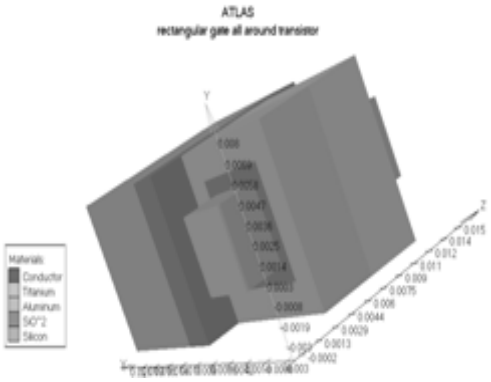

Figure.1 3D view of a dual metal square surrounding gate MOSFET.

3. Results

Our results have been validated using numerical simulation that is an extremely helpful tool for detailed investigation of physical phenomena, which determine electrical characteristics of semiconductor devices [8],[9]. In this study Atlas Silvaco Software has been chosen [10]. The simulated output and transfer characteristics of the GAA device considered are plotted in figures 2 and 3.

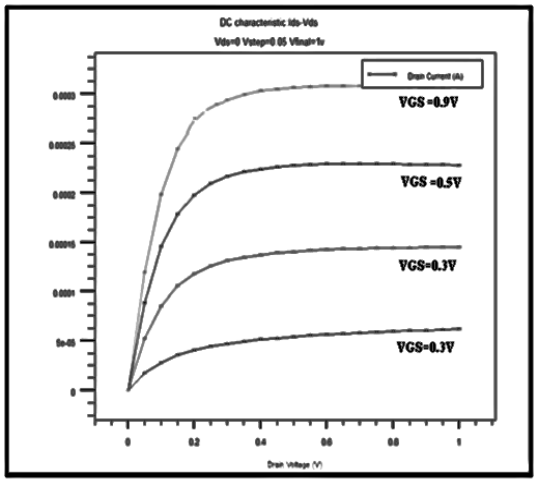

Figure. 2 ID versus VD characteristics

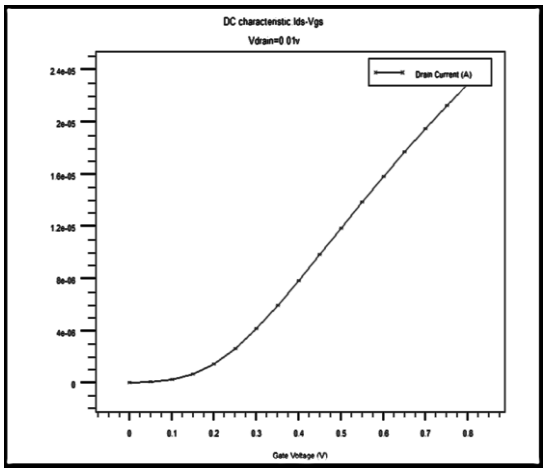

Figure.3 Transfer characteristic

Figure 2 shows IV characteristics of our square GAA with n-type semiconducting channel at different positive gate bias. In contrast, Figure 3 shows transfer characteristic of our device. Threshold voltage can be extracted from this figure knowing that physically, the threshold voltage is defined as the gate voltage that is required for creating a conducting channel and allowing the carriers to flow from the electrode source to the drain crossing this conducting channel. In our case threshold voltage extracted Vth is equal to 120mV. In order to study the influence of the studied structure parameters on our device electrical characteristics, some physical and geometrical

parameters are modified. We examine then the effect of each parameter variations on our GAA transistor drain current and threshold voltage .

3.1. Influence of Tox variation on ID current and threshold voltage Vth

Figure 4 shows our device output characteristics at different oxide thickness.

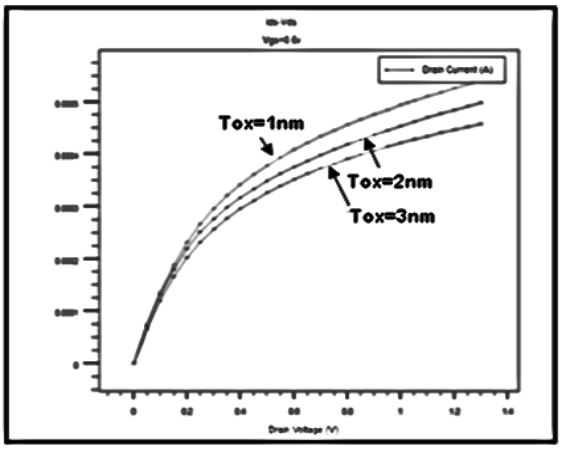

Figure.4 Output characteristics for a dual metal gate GAA MOSFETs at different oxide thickness (Tox=1nm, 2nm, 3nm).

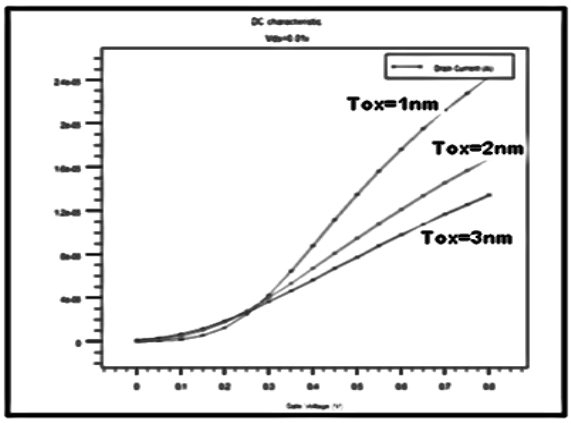

Figure.5 Transfer characteristics for a dual metal gate GAA MOSFETs at different oxide thickness (Tox=1nm, 2nm, 3nm).

We can observe that drain saturation current increases at shorter oxide thickness. We can conclude for this variation that thinner gate oxides lead to product higher drain currents. Figure 5 allows showing that threshold voltage also depends on oxide thickness.

3.2. Influence of channel length (Lch) variation on ID current and threshold voltage

Simulation results allowing to investigate the effects of channel length on I_{DS} current are presented in figures 6 and 7.

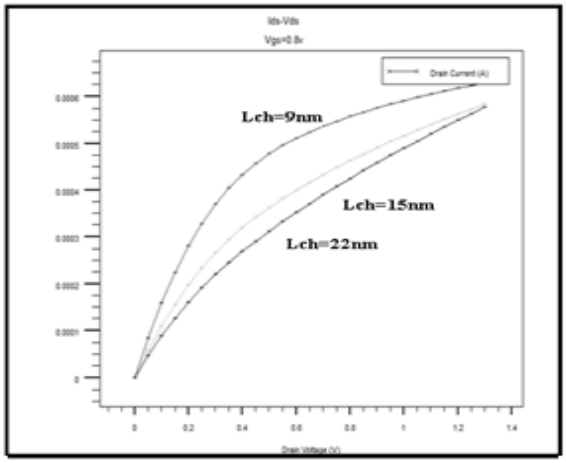

Figure.6 Output characteristics for a dual metal gate GAA MOSFETs at different channel length (Lch=9nm, 15nm, 22nm).

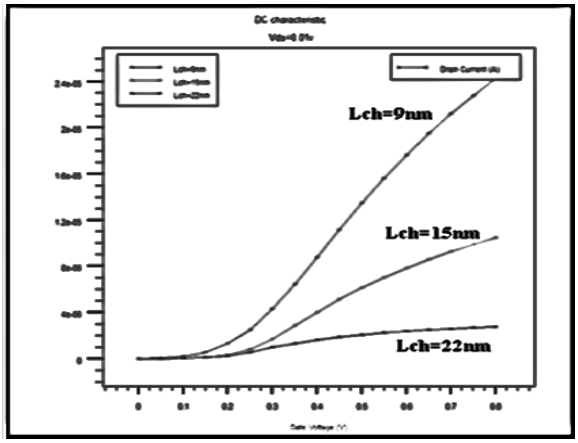

Figure7. Transfer characteristics for a dual metal gate GAA MOSFETs at different channel length (Lch=9nm, 15nm, 22nm).

As shown in Figure 6, the drain I_{DS} is inversely related to the channel length. Thereby, when Lch increases the drain currents increases and threshold voltage decreases too.

3.3. Influence of oxide layer type on ID current and threshold voltage Vth.

The introduction of high-k gate oxide in 2007 was a breakthrough in microelectronics as Intel developed 45nm technology processors with hafnium based material as gate dielectric. Nowadays several high-k materials ranging from Al2O3 to perovskites are being vigorously investigated, in order to identify a long term promising material. In this part of our study two gate dielectric, those are HfO2 and Si3N4, are used and compared to conventional gate oxide SiO2.

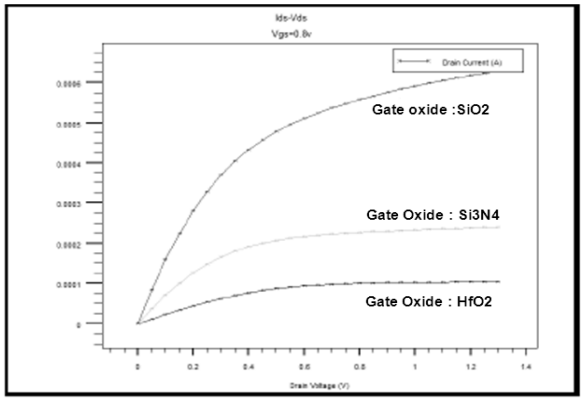

Figure..8 Output characteristics for a dual metal gate GAA MOSFETs at different High-k dielectric type (SiO2, Si3N4 and HFO2).

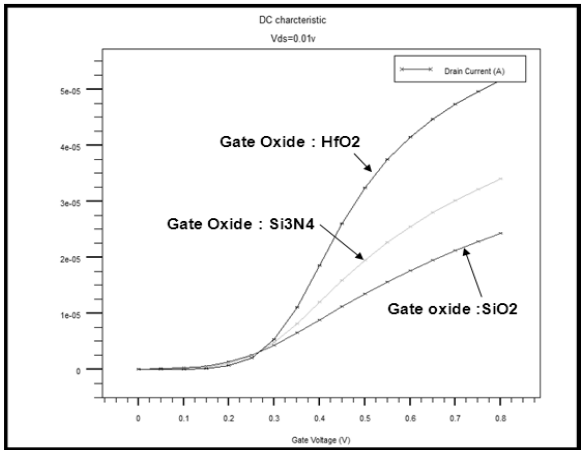

Figure. 9. Transfer characteristics for a dual metal gate GAA MOSFETs at different type of oxide (SiO2, Si3N4 and HFO2).

Figure8 and Figure9 allow to observe the impact of gate dielectric on our device electrical characteristics. With the integration of high-k dielectrics Into GAA SOI MOSFETs, the performance of the device are supposed to be further enhanced and improved and this can be achieved using a sacrificial SiO2 layer with a high k gate dielectric.

3.4. DIBL (Drain Induced Barrier Lowering) and Ion/Ioff ratio

The DIBL (Drain Induced Barrier Lowering) piercing said phenomenon which occurs when the dimensions of defected areas (ZCE) source / substrate and drain / substrate become comparable to the gate length. The potential distribution in the channel depends on both of the transverse field (controlled by the gate voltage), and the longitudinal field (controlled by the drain voltage) leading to drain side ZCE increasing, which causes the lowering of the barrier of source / substrate potential.

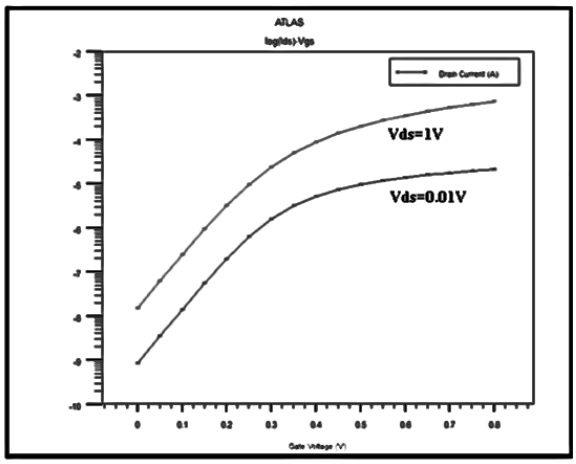

Figure.10. Highlighting of DIBL effect.

The DIBL parasitic effect appears in short channel transistors. This effect is principally due to the fact that in the weak inversion regime, there is a potential barrier between the channel region and the source. The height of this barrier is a result of the balance between drift and diffusion current between source and channel regions. If a high drain voltage is applied, the barrier height decreases leading to drain current increasing. Consequently the drain current is controlled not only by the gate voltage, but also by the drain voltage. The DIBL effect is apparent when we observe the transfer curves of our transistor for

the linear and saturated cases as shown in figure 10. In fact in the case where there is no DIBL, the two curves would match in the subthreshold regime.

The DIBL effect can be measured by the lateral shift of the transfer curves in the subthreshold regime divided by the drain voltage difference of the two curves and is given in units (mV/V). It can be expressed by:

$$DIBL = \frac{\Delta V_{TH}}{\Delta V_D}(mV/V) \quad (1)$$

From the equation 1 and Figure10 our device DIBL extracted is equal to $39mV/V$.

4. Conclusion

The downward revision of bulk planar MOSFET according to the International Technology Roadmap sheet for Semiconductors ITRS requires new structures such as MOSFETs gate all around (GAA MOSFETs). These structures can reduce short channel effects that appear below 10nm node. The structure studied in this paper is a Dual Metal Square surrounding Gate MOSFET. It has been found that the GAA MOSFETs have very good SCE immunity and are suitable to be used for low voltage low power applications Based on the simulation results we have obtained using SILVACO software, appropriate parameters can be chosen to optimize our structure.

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